# Dynamic Stability and Noise Margins of SRAM Arrays in Nanoscaled Technologies

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***Abstract*—SRAM stability is one of the primary bottlenecks of current VLSI system design, and the unequivocal supply voltage scaling limiter. Static noise margin metrics have long been the de-facto standard for measuring this stability and estimating the yield of SRAM arrays. However, in modern process technologies, under scaled supply voltages and increased process variations, these traditional metrics are no longer sufficient. Recent research has analyzed the dynamic behavior and stability of SRAM circuits, leading to dynamic stability metrics and dynamic noise margin definition. This paper provides a brief overview of the limitations of static noise margin metrics and the resulting dynamic stability and noise margin concepts that have been proposed to overcome them.**

***Index Terms*—SRAM, Static Noise Margin, Dynamic Noise Margin, Stability Analysis, Separatrix, Phase Portrait**

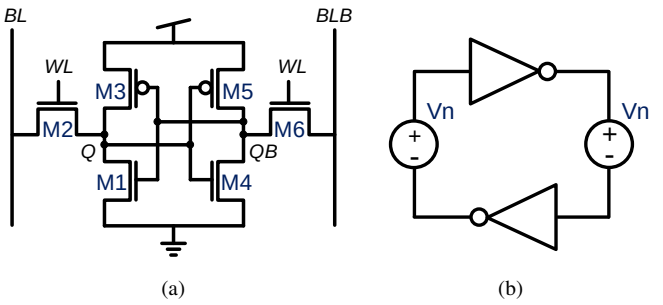



Fig. 1. (a) Schematic of a standard 6T SRAM bit cell. (b) DC Voltage Noise concept of Static Noise Margins.

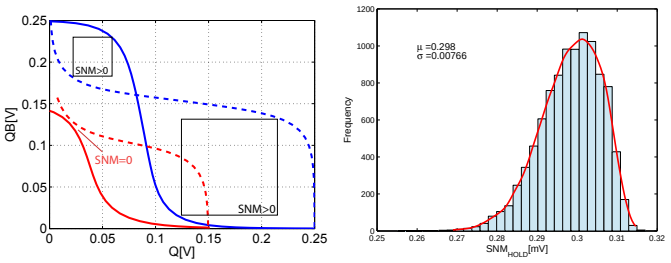
## I. Introduction

Ever since VLSI minimum feature scaling passed sub-micron dimensions and penetrated into the deep-nanoscaled era, the stability of static random access memory (SRAM) has been a pressing issue. In the past, the pursuit of high-frequency operation led to relatively slow voltage scaling, resulting in high noise margins for ratioed circuits, such as the six-transistor (6T) SRAM cell (Fig. 1(a)). However, the limits on power density [1] have led to significant supply voltage ($V_{\mathrm{DD}}$) scaling. As the gap between $V_{\mathrm{DD}}$ and the transistor threshold voltage ($V_{\mathrm{T}}$) decreased in order to limit costly sub-threshold leakage currents, the previously sufficient noise margins have dropped to problematic levels. For SRAM cells, this has become critical, as these cells are generally designed with minimum features, adhering to special "pushed design rules", resulting in even smaller margins and high susceptibility to process variations. Due to the fact that these circuits generally appear millions of times on a single integrated circuit, these process variations, which increase as the channel length scales and fabrication processes become more complex, have a high probability of causing failures. For several years, SRAM blocks have been recognized as the limiting components in system supply voltage scaling, rarely enabling operation below 800 mV. Aggressively scaled, low power systems, often connect these arrays to a separate, higher supply, resulting in costly overhead and undesirable power consumption. Alternatively, advanced circuit techniques, redundancy, error correction, and other "guardbanding" mechanisms are introduced, trading off performance, silicon area, and power, for reduced failure rates. However, in order to truly guarantee robust performance, and in addition, limit the overhead and power consumption of guardbanding, accurate analysis and comprehension of the actual circuit noise margins is essential.

Failures in SRAM circuits are generally attributed to four primary failure mechanisms [2]:

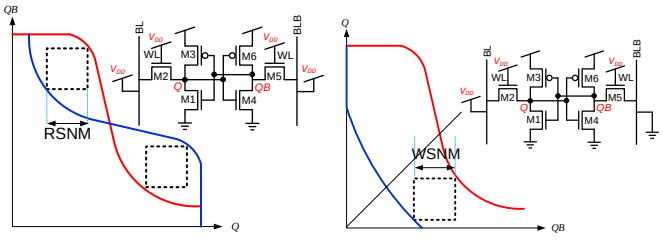
- *Hold Failures* - The inability of the cell to store a given data state or a data flip caused by a single-event upset (SEU), such as a particle strike or coupling noise from a neighboring signal.
- *Write Failures* - The inability to write a certain data state into a bitcell.
- *Read Failures* - A data flip caused during a cell read access. This category also can include *Half-Select Failures*, which occur when data is written to other cells that share the same wordline.
- *Access Failures* - A wrong data level read out of a cell due to the inability of the cell to correctly drive the output circuitry (generally the bitlines and sense amplifier) within the chosen access time.

For all but the access failures, the traditional method to measure failure probability has been the well known Static Noise Margin (SNM), well defined by Seevinck in his groundbreaking paper from 1987 [3]. The SNM metric assumes a DC voltage noise applied in opposite polarities to the two internal data nodes (Q and QB of Fig. 1(a)) of the 6T SRAM cell. This figure-of-merit (FOM) enables fast, simple, and straightforward extraction of a single number to define




(a) (b)

Fig. 2. (a) Butterfly curves of 6T SRAM under local mismatch at 400 mV (bi-stability maintained) and 250 mV (loss of bi-stability).




(a) (b)

Fig. 3. Circuit simulation setup and resulting butterfly curves for (a) RSNM measurement. (b) WSNM measurement.

noise margins and hold failure probability, and can be easily modified to cover read and write failures, as well. However, its static nature fails to capture the inherent dynamic behavior of the 6T SRAM cell and access operations. In order to capture the true dynamic nature of SRAM bitcell and array operations, and thereby design more robust components with smaller guardbands, new dynamic stability methods and metrics have been introduced. The following sections will provide a brief overview of dynamic stability theory and metrics, as described in recent publications.

## II. Static Noise Margins and its Limitations

The underlying assumption of the traditional SNM metric is that in a worst-case scenario, two voltage sources of magnitude $V_n$ with opposite polarities are connected to the internal data nodes, as shown in Fig. 1(b). The 6T circuit can withstand such an attack and still retain its initial value, as long as its inherent bi-stability is maintained. This can be both illustrated and measured graphically through the well-known *butterfly curves* that plot the voltage transfer characteristics (VTC) of the circuit's feed-forward and feed-back inverters on a single plot. The SNM FOM is the largest value of $V_n$ that the circuit can tolerate without becoming mono-stable. To illustrate this, butterfly curves of a 40 nm 6T SRAM bitcell under two aggressively scaled supply voltages are plotted in Fig. 2(a). Bi-stability is maintained with under a 250 mV supply, but when the voltage is reduced below 150 mV, the circuit becomes mono-stable, and therefore can only store a logic '1' (Q=$V_{\mathrm{DD}}$, QB=0 V). The asymmetry of the plots in Fig. 2(a) is caused by process variations, which make one of the internal inverters stronger than the other.

While there is no physical equivalent of a serial DC voltage noise, as assumed by the SNM metric, it provides a legitimate model for distortions to compare the robustness of several storage cell topologies. Moreover, a *negative* SNM implies that the circuit is mono-stable by design, and therefore a hold failure is guaranteed to occur, even under noise-free conditions. Therefore, a mandatory measurement for the reliability of an SRAM cell is a low probability for a negative SNM under process variations, often extracted through statistical Monte Carlo (MC) simulation, as shown in Fig.2(b). Yield estimation for SRAM bitcells is achieved through the mean-to-variance ($\mu/\sigma$), where a figure of 6–8$\mu/\sigma$ often is used to set the minimum data retention voltage (DRV), ensuring many millions of samples per failure. Similar methods can be used to plot the distributions of read SNM (RSNM) and write SNM (WSNM) to predict read failure and write failure probabilities by biasing the circuit-under-test with its access voltages. Alternative methods for extraction of WSNM and RSNM, such as the N-curve [4] and bitline sweep [5] methods, have also been proposed to overcome some of the limitations of the Seevinck method. However, all of these are inherently static in nature, and therefore fail to capture the dynamics of the SRAM bitcell and its access operations.

### *Hold SNM Limitations*

The first limitation of SNM is its failure to properly define resilience to SEUs, such as particle strikes at high altitudes [6] or cross coupling from toggling of adjacent nets. These events generally inject or remove charge from the bitcell's parasitic capacitors causing a voltage step at the data nodes. However, as opposed to the underlying assumption of SNM, this voltage change is temporal and shaped, causing a very different reaction and result than a static voltage level. In addition, due to the close proximity of the internal data nodes, these disturbances are most often of the same polarity, as opposed to the SNM assumption of opposite polarity noise attacks, leading to an over-pessimistic estimation. Finally, there is no accurate method to convert such a charge injection/removal into a bi-polar voltage step, such that the actual number provided by the SNM metric provides a good means for relative comparison, but cannot show the ability of a bitcell to withstand a particular strike or provide a failure probability within a given environment.

Similar limitations are relevant when discussing RSNM and WSNM; albeit, in these cases, the entire operation has a temporal component. Both of these operations are activated according to pulsed signals, whereas SNM is a pure DC analysis. Furthermore, RSNM provides a pessimistic failure probability estimation leading to very pessimistic guardbands, while WSNM leads to an optimistic estimation, which could lead to lower yield.

### *Read SNM Limitations*

The RSNM metric is measured by applying a static $V_{\mathrm{DD}}$ bias to both the wordline and bitlines (WL, BL, and BLB),

as illustrated in Fig. 3(a). In reality, WL is pulsed with a given waveform and BL/BLB are pre-charged to $V_{\mathrm{DD}}$ and subsequently floated. Several important phenomena are ignored with the RSNM setup. First, during both assertion and de-assertion of the WL, coupling and charge injection cause a voltage step at Q and QB. Second, during the read operation, either BL or BLB is partially discharged, lowering the drain-to-source ($V_{\mathrm{DS}}$) voltage over the respective access device (M2 or M6). Finally, the duration of the read pulse is limited, such that the dynamic voltage change at the internal data nodes is suddenly disrupted at the conclusion of the read access time ($T_{read}$). Therefore, the trip point, at which the bi-stability of the cell is lost and the cell could flip, may never be reached during an actual read access. Hence, the RSNM metric, which assumes an infinite read time, could predict a higher read failure probability than possible during an actual WL pulse, leading to over-design. Alternatively, severe cross-coupling could lead to a flip during WL assertion, leading to missed failures, not captured by RSNM.

*Write SNM Limitations*

The WSNM metric is similarly measured by biasing the control signals at constant voltages, with WL high and BL/BLB oppositely driven according to the data to be written, as illustrated in Fig. 3(b). Whereas in this case, the bitlines actually are driven to their appropriate biases, the wordline access is again temporal. Similar cross-coupling and charge-injection phenomena occur, as well as the abrupt cessation of the internal voltage changes due to de-assertion of WL. In this case, however, the major concern is that the write access time ($T_{write}$) is too short to flip the circuit into the opposite stable state, thereby erroneously maintaining its data. This is entirely overlooked by the WSNM metric, as the write pulse is assumed to be infinite. An example of such a write failure that would be missed by the WSNM metric is illustrated in Fig. 4. In addition, the actual trip point of a cell is susceptible to variation (i.e., Q>QB is not a sufficient threshold to assume the final state of the cell will be Q='1', QB='0'), leading to an often overlooked, non-trivial decision as to where the maximum square measurement should be made and resulting in inaccurate WSNM extraction from many of the static methods.

A final, albeit very acute, limitation of SNM metrics is their failure to appropriately evaluate the stability of alternative, complex bitcells that do not adhere to the standard dual-data node, static operation of the 6T bitcell, or employ non-standard access patterns. Recent examples of such cells gate the supply during write access [7]; have more than two internal data nodes [8], [9]; operate under dynamic or quasi-static topologies [8], [10], [11]; or employ portless operation [12]. In these cases, alternative metrics are required for stability analysis and failure probability estimation.

## III. Dynamic Stability and Dynamic Noise Margins

The concept of dynamic stability of SRAM cells is rather straightforward. Starting with an initial logic state, an event

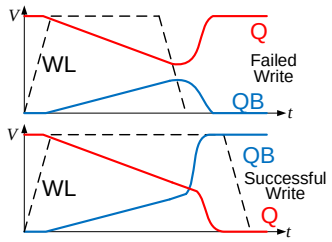



Fig. 4. Illustration of a successful and failed write operation, according to the write access time.

is applied to the SRAM cell – be it a cell access (read or write) or a noise event (SEU). Following the completion of the event, if the state of the cell is as expected (the same as before for hold and read or flipped for write), the cell is found to be dynamically stable [13]. Estimation of dynamic stability is generally done at both a single cell level for fast, many sample statistical (MC) simulations, and at a full block level for thorough analysis that takes into consideration all factors. However, full system simulation requires very slow and complex transient simulations; hence high-yield estimation is usually only possible through advanced statistical estimation techniques, such as sensitivity analysis, most probably failure point [13], [14], importance sampling [15], and statistical blockade [16]. In today's SRAM design, application of these techniques is mandatory. However, as opposed to the traditional SNM metric that provides a number that quantifies *how stable* a given sample is, dynamic stability estimation only provides a "pass" or "fail" result. This may be sufficient for yield estimation and for reaching decisions on integration of redundancy and error correction techniques; however, it provides very little insight on *why* the circuits are failing, *how close* they are to failure in light of noise or other parameter fluctuations, and consequently, how to improve the design.

In order to provide the designer with better tools for improvement, similar to those provided by the SNM metrics and butterfly curves, the concept of dynamic noise margins (DNM) was introduced. Its origin dates as far back as Lostroh's paper from 1979 [17]; however the first true methodology for DNM definition and extraction was given by Ding, et al. in 2004 [18]. Based on the conventional SNM methodology, Ding proposed plotting the *dynamic VTCs* (DVTC) of logic gates with the DNM defined as the maximum square that fits into the resulting quasi-static butterfly curves. This definition of DNM provided a dynamic metric for logic gates that was analogous to the textbook noise margin definition [19], but was not effective in capturing the dynamics of SRAM bitcells, especially under read and write accesses.

Huang's group at Texas A&M [20] proposed several simulation methods for analyzing the dynamic stability of SRAM cells. Noise events were modeled as a current source injecting charge into one of the cell's internal data nodes. Due to the symmetry of a 6T cell, this setup is sufficient for modeling noise caused by coupling or particle strikes, depending on the waveform of the current pulse. The state of the internal nodes

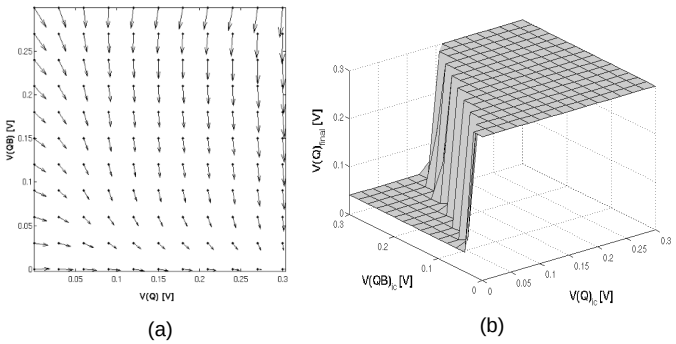



Fig. 5. (a) Phase portrait of a successful write '1' operation at $V_{\mathrm{DD}}$ =300 mV. (b) State space plot of a failed write '1' operation at $V_{\mathrm{DD}}$ =300 mV under extreme process variations.

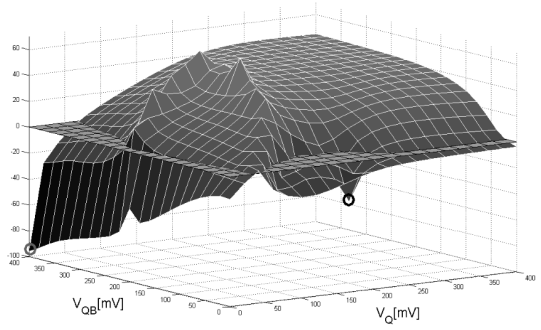



Fig. 6. Loop gain of a QSRAM bitcell at 400 mV, showing two stable equilibrium.

throughout a transient simulation is plotted as the *trajectory* of the circuit. Depending on the amplitude and duration of the noise source (assuming a square current pulse), the cell either flips or maintains its state. In addition, initial SRAM state-space analysis was presented.

These concepts were extended by the same authors in [21]. State space analysis was again employed to plot the *phase portrait* of the 6T bitcell, showing two distinct equilibria, coinciding with the bitcell's bi-stable logic states. Following a noise event, the state of the bitcell will reside in the region-of-attraction of one of these equilibria, and thereby be pulled towards it and eventually settle at this logic state. The stability boundary that separates these regions-of-attraction is called the *separatrix*. Whereas, in a completely symmetric cell, the separatrix separates the state-space exactly on the 45° Q=QB line, the authors show that in the presence of device mismatch, this boundary can significantly deviate, and therefore, they derive an efficient algorithm for tracing the separatrix. Further state space modeling, including analysis of phase portraits during write operations was provided in [22]. Examples of this analysis are provided in Fig. 5, demonstrating a phase portrait under a write operation (Fig. 5a) and a three-dimensional state-space plot of a failed write operations (Fig. 5b).

The leading definition of dynamic noise margins was provided by Huang's group in [23], measuring the time it takes for the internal state of the SRAM cell to cross its separatrix ($T_{across}$). For read accesses, crossing the separatrix results in a read failure and therefore, read DNM is defined as the time difference between maintaining and losing state:

$$DNM_{read} = T_{across} - T_{read}. \tag{1}$$

Alternatively, for a write access, flipping the state is the goal of the operation, and therefore write DNM is defined as:

$$DNM_{write} = T_{write} - T_{across}. \tag{2}$$

An alternative, albeit similar, definition of write DNM was proposed by Calhoun's group at Virginia [5]. In this analysis, write operations are modeled by connecting a current source to each internal node, each with a piece-wise linear model of the actual current waveforms simulated during a standard write access.

Sharifkhani and Sachdev [24] provided extensive control-theory analysis of an SRAM cell as a non-linear circuit, defining dynamic SNM ($SNM_D$) as a superset of traditional SNM. This work includes analysis of SRAM dynamic stability under sub-threshold supply voltages, and loop gain analysis is proposed as an additional design tool to examine stability. This tool was employed to demonstrate the stability of a quasi-static SRAM (QSRAM) bitcell at subthreshold voltages in [8], as show in Fig. 6.

A blackbox stability analysis framework was proposed in [25], providing an improved algorithm for phase-portrait and separatrix extraction, as well as a new metric for characterizing cell robustness. This metric, called separatrix affinity, is rooted in the idea that overall failure probability of a cell can be correlated to the readiness of one of its stable states to cross the separatrix. This method provides the designer with insight as to the sensitivity of the dynamic stability of the cell to various cell parameters.

## IV. Conclusions

This paper presented a brief overview of Static and Dynamic Stability and Noise Margins of SRAMs cells. It was shown that the traditional static noise margin metrics for estimating stability and failure probabilities are no longer sufficient in deeply nanoscaled process technologies. Therefore, recently derived dynamic stability and noise margin concepts are essential for analysis and qualification of SRAM blocks in modern systems. Several techniques and methodologies have been proposed to provide the SRAM designer with tools to evaluate dynamic stability. However, due to the relative immaturity of this theory, there has yet to be a clear-cut winner as to the de-facto standard for stability analysis and dynamic noise margin definition and characterization.

## Acknowledgements

Dr. Teman is supported by a Swiss Government Excellence Scholarship. I would like to thank Prof. Andreas Burg, Prof. Alexander Fish, Mr. Robert Giterman, and Mr. Anatoli Mordakhay for their assistance in preparation of this work.

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